Abstract of the Disclosure

A memory array has memory elements of identical topology or footprint arranged in rows and columns. 5 of the memory elements are EEPROM cells and other memory elements are read only memory cells but all are made using a mask set having the same length and width dimensions. In the mask set for EEPROMs a principal mask is used for formation of a depletion implant. case of one type of read-only memory element, this mask 10 is mainly blocked, leading to formation of a transistor with a non-conductive channel between source and drain. In the case of another read only memory element, the same mask is unblocked, leading to formation of a transistor 15 with a highly conductive or almost shorted channel between source and drain. These two read only memory elements are designated as logic one and logic zero. By having rows of read-only memory elements with rows of EEPROMs on the same chip, a more versatile memory array 20 chip may be built without sacrificing chip space.